

Abstract for: SPIE International Symposium on Remote Sensing, 17-21 September 2001  
Toulouse, France

**Advances in 2nd Generation, Ultra-Low Power CMOS Active Pixel Sensor imagers for Remote Sensing, Star Tracking, Optical Comm and Low-Cost Solar Array/Antenna Boom Deployment Metrology**

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**Abstract:** In recent years, JPL has implemented advances in CMOS APS visible sensor design that have produced a technology well suited for the development of ultra-low power, miniature, highly integrated image sensor systems. Remote sensing and flight applications currently being proposed and implemented for these relatively low-cost, easily integrated, modular high performance "camera-on-a-chip" sensors include their use as: remote earth and planetary sensing cameras, solar array and/or antenna deployment sensors, star trackers and high bandwidth optical communication beacon tracking focal plane arrays. This paper reports on these new advances in design and remote sensing implementation of the newest generation of CMOS APS dubbed the Versatile Integrated Visible Imager or VIDI APS "camera-on-a-chip".

The newest generation of digital integrated camera design at JPL is a 512 x 512 format and utilizes 12-um pixels. The chip size is 10 mm x 15.5 mm. Features include all digital interface, 512-column parallel, analog or 10-bit ADC digital output, on-chip timing and control, and on-chip bias generators using four five-bit DACs. The new 512 VIDI chip also provide a "five-wire" interface. The chip, fabricated on a standard foundry, uses 0.6 um design rules allowing 3.3 V supply. VIDI offers programmable resolution, data efficient "smart" area-of-interest windowed high speed readout, no blooming, and exposure while continuing to operate with ~ 20 mW of power in the on-state and ~ 40 uW in the "sleep" state. The chip uses a rolling shutter and has a maximum data rate of the chip is 10 Mbits/sec.

**Author Bio:** Dr. Robert Stirbl is a Senior Member of the Engineering Staff in JPL's Advanced Imager and Focal Plane Technology Group and has 30 years of academic and industrial experience with electro-optical system for AT&T, Allied-Bendix, Northrop-Grumman, and Riverside Research Institute. He has designed, and managed the development of several space remote sensing and optical metrology systems. Dr. Stirbl has published over fourteen papers, and he holds 12 US patents. He is currently manager for several government agency programs to adapt Ultra-low power, "sensor-on-a-chip" CMOS imagers for DoD, NASA, medical, and industrial applications.